1. A two transistor flash memory cell, comprising:

a) a floating gate storage device with a shallow N+ source region,

b) an access device with a shallow N+ drain region,

c) said storage device and said access device share a shallow N+ common region that is a drain for the storage device and a source for the access device,

d) said source, drain and common regions producing a symmetrical memory cell in which size of the memory cell is limited by characteristics of a read operation.

2. The memory cell of claim 1, wherein the storage device and the access device are NMOS devices.

3. The memory cell of claim 1, wherein the floating gate storage device is coupled in series with the access device to form a cell to create a compact flash array for programmable logic devices.

4. The memory cell of claim 1, wherein a channel erase operation using Fowler-Nordheim (FN) tunneling is used to erase said floating gate storage device and a channel program operation using FN tunneling is used to program said floating gate storage device.

5. The memory cell of claim 4, wherein the channel erase operation decreases a threshold voltage of said floating gate storage device and the channel program operation increases the threshold voltage of said floating gate storage device.

6. The memory cell of claim 4, wherein a low voltage gradient is produced from source to drain of the storage device during the channel program operation which allows a shorter channel length for high density applications.

7. The memory cell of claim 1, wherein said source region, said drain region and said common region are located in a P-well, within a deep N-well on a P-substrate.

8. The memory cell of claim 1, wherein said source region, said drain region, and said common region are located on a P-substrate.

9. The memory cell of claim 1, wherein a tunnel oxide of said storage device and a gate oxide of said access device are created within a same process step.

10. The memory cell of claim 1, wherein a floating gate of said storage device and a gate of said access device are formed within a same process step.

11. A flash memory array for use in high density and low voltage applications, comprising:

a) an array of two transistor flash memory cells, comprising a storage transistor and an access transistor arranged in rows and columns and formed with cells containing a floating gate storage device and an access device,

b) said cells in a column are coupled by bit lines and source lines,

c) said bit lines are decoded by a bit line decoder and said source lines are decoded by a source decoder,

d) said cells in a row are coupled by word lines and access lines,

e) said word lines are couple to control gates of said storage devices and are controlled by a word line decoder,

f) said access lines are coupled to gates of said access devices and are controlled by an access decoder.

12.The flash memory array of claim 11, wherein the two transistor memory cells are arranged such that channels of said storage transistor and said access transistor are oriented vertically.

13. The flash memory array of claim 11, wherein said bit lines are segmented metal lines that couple drains of said access transistors in said column of memory cells, and said source lines are segmented metal lines that couple sources of said storage transistors in said column of memory cells.

14. The flash memory array of claim 11, wherein an erase operation erases a block of memory cells simultaneous using a Fowler-Nordheim channel erase operation to remove electrons to a floating gate of said memory cells and thereby decreasing a threshold voltage of said block of memory cells.

15. The flash memory array of claim 11, wherein a program operation programs memory cells using a Fowler-Nordheim channel program operation to add electrons to a floating gate of said memory cells and thereby increasing a threshold voltage of said block of memory cells.

16. The flash memory array of claim 11, wherein erase and program operations are performed without any verification.

17. The flash memory array of claim 11, wherein memory cells that are not selected for a memory operation are biased to eliminate disturb conditions.

18. A low voltage high density nonvolatile memory cell, comprising:

a) a nonvolatile storage means,

b) an access means,

c) said storage means coupled to said access means,

d) said access means providing access to data stored in said storage menas.

19. The nonvolatile memory cell of claim 18, wherein the nonvolatile storage means and the access means are couple in series and share an N+ region located in a P-well within a deep N-well on a P-substrate.

20. The nonvolatile memory cell of claim 18, wherein access means provides access to said nonvolatile storage means.

21. The nonvolatile memory cell of claim 18, where said storage means is programmed using Fowler-Nordheim channel tunneling means and is erased using Fowler-Nordheim channel tunneling means.

22. The nonvolatile memory cell of claim 18, wherein the storage means and the access means are produced using a same process.

23. A nonvolatile memory array, comprising:

a) a memory cell means comprising a nonvolatile storage means and an access means.

b) a memory array means configured with said memory cell means,

c) a column of cells of said memory array means coupled to access means of said column of cells by a bit line means and coupled to nonvolatile storage means of said column of cells by a source line means,

d) a row of cells of said memory array means coupled to access means of said row of cells by an access line means and coupled to nonvolatile storage means of said row of cells by a word line means.

24. The nonvolatile memory of claim 23, wherein said nonvolatile storage means and said access means are coupled by an N+ implantation means locate in a P-well with a deep N-well on a P-substrate.

25. The nonvolatile memory of claim 23, wherein said nonvolatile storage means and said access means are coupled by an N+ implantation means locate on P-substrate.

26. The nonvolatile memory of claim 23, wherein said bit line means is formed by segmented means of metal lines.

27. The nonvolatile memory of claim 23, wherein said source line means is formed by segmented means of metal lines,

28. The nonvolatile memory of claim 23, wherein said bit line means is controlled by a bit line decoder means.

29. The nonvolatile memory of claim 23, wherein said source line means is controlled by a source line decoder means.

30. The nonvolatile memory of claim 23, wherein said access line means is controlled by an access line decoder means.

31. The nonvolatile memory of claim 23, wherein said word line means is controlled by a word line decoder means.

32 The nonvolatile memory of claim 23, wherein said cells are programmed using Fowler-Nordheim channel tunneling means, and said cells are erased using Fowler-Nordheim channel tunneling means.

33. A method for creating a nonvolatile memory for a low voltage and high performance applications, comprising:

a) forming an array of nonvolatile memory cells, wherein each cell comprises a nonvolatile storage device and an access device,

b) coupling said memory cells in a column of said array to bit lines and to source lines,

c) coupling said memory cells in a row of said array to word lines and access lines,

d) selecting said memory cells with said bit lines and said source lines,

e) accessing said memory cells with said word lines and said access lines.

34. The method of claim 33, wherein said memory device and said access device are coupled by an implanted N+ region in a P-well within an N-well on a P-substrate.

35. The method of claim 33, wherein said memory device and said access device are coupled by an implanted N+ region on a P-substrate.

36. The method of claim 33, wherein said cells in a column are coupled to said bit line through a drain of said access devices of each cell in the column.

37. The method of claim 33, wherein said cells in a column are coupled to said source line through a source of said storage device of each cell in the column.

38. The method of claim 33, wherein said cells in a row are coupled to said access line through a gate of said access device of each cell the row.

39. The method of claim 33, wherein said cells in a row are coupled to said word line through a control gate of said access device of each cell in the row.